DC power quality standardization status

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KEY FIGURES 23-24 FOR R&D

1,800 employees in France

31% of women

282 outside France

14% of employees are under the age of 30

more than **250** research teachers

160 PhD students

44 nationalities

9 research centers in France and abroad

more than **300** academic and industrial partnerships

11 petaflops of computing capacity

more than **70** testing platforms

21 joint laboratories

512 M€ budget in 2023

EDF

EDF R&D 2023 2024 OUR ACTION

Expertise in all areas of the low carbon energy sector

The opening to a group with **160,000** employees worldwide

2,178 patents

400 R&D projects conducted in 2022

99% of operating budgets dedicated to decarbonisation and transition of energy systems

300 scientific papers

220 expert and senior researchers with a high level of expertise on a national or international scale

5 million X views

45 initiatives with schools/universities (forums and school visits)

97% satisfaction expressed by R&D clients

17.6 million of euros from services sales or grants

Agenda

1. Standardization activities in IEC

2. 9kHz-150kHz Quasi-Peak data processing

1

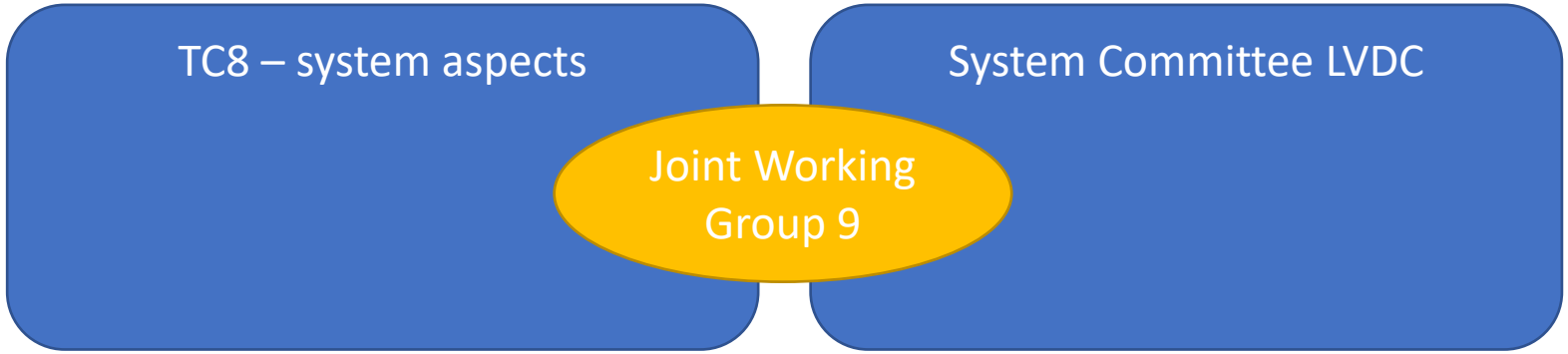
Standardization activities in IEC

Focus on DC power quality topics

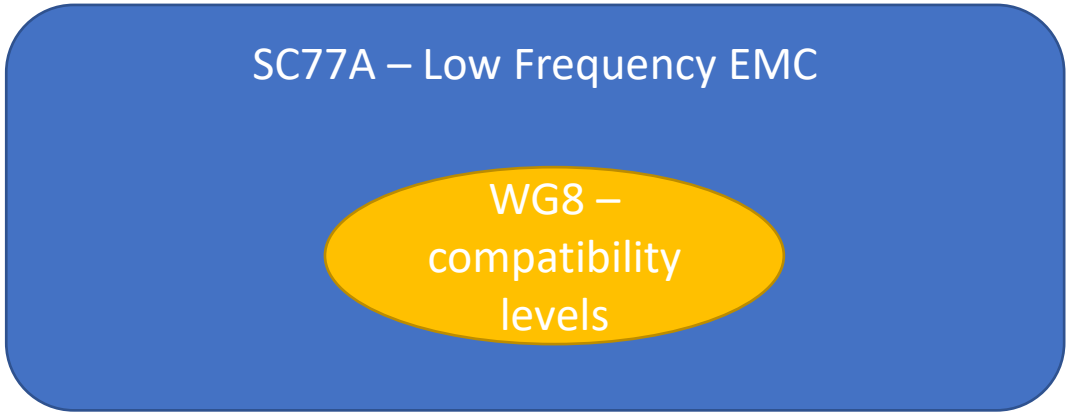
Power Quality in IEC technical committees

International Electrotechnical Commission

On-going work



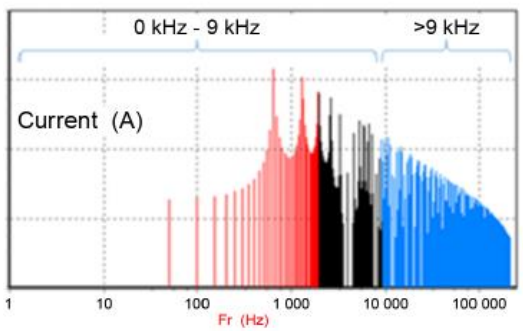
Future work

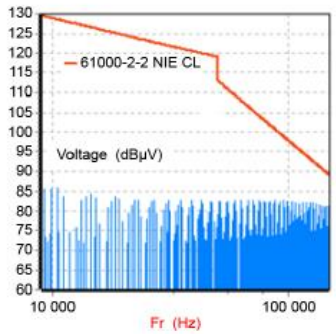


And ongoing work in TC13, TC85 focused on metering

Circulated to national committees in feb 2024

IEC TC8/JWG9: DTR 63282 ED2- LVDC systems - Assessment of standard voltages and power quality requirements (ed.2)





Compatibility Levels definition in SC77A/WG8

Compatibility levels are the first brick to define **emission** limits and **immunity** thresholds to achieve electromagnetic compatibility between devices

IEC SC77A/WG8: 2024-02-16, circulation of Questionnaire: Proposal regarding the definition of compatibility voltage levels for LVDC networks

1- What problems will be solved by developing compatibility levels for DC grids?
2- What are the failure mechanisms expected for DC equipment and DC systems?
3- Do you have examples of electric parameters or immunity issues related to DC systems and equipment?
4- What DC disturbance phenomena are encountered? Voltage variation, voltage sag, unbalance, frequency spectra, etc.?
5- What type of DC networks shall be considered (e.g. inductive/capacitive, single polar/bi-polar, IT/TN, residential/commercial/industrial, public/private, voltage levels, total power, etc.)?
6- Is there any other EMC phenomena or additional information related to DC grids you are willing to share?

Next stage: Analyse of feedbacks from NCs for further actions

2

CISPR 16 Quasi-Peak assessment

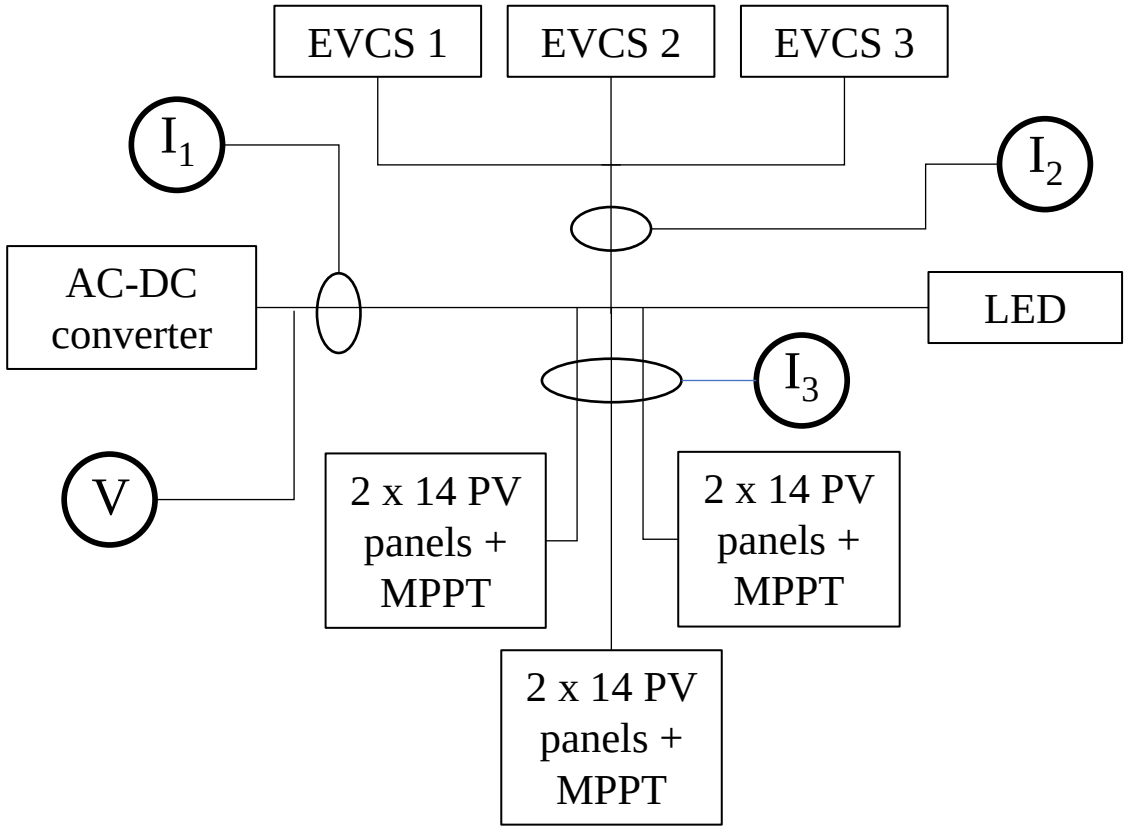
Data processing in 9kHz-150kHz of in-situ recordings

Data processing of data of the ASR building in Utrecht

About 2 hours of recordings

Processing of the voltage and currents with **Digital-CISPR** implementation to be in-line with IEC 61000-2-2 compatibility levels in AC grids between 9kHz and 150kHz (**Quasi-Peak** detector with 200Hz resolution), with a time-domain aggregation of 3s.

Processing done in Matlab with a script compliant with committee draft of IEC 61000-4-30 ed4 (not publicly available)



What is quasi-peak ?

IEC 61000-2-2 (compatibility levels for **AC** grids in **residential** environment):

« The compatibility levels for voltage distortion in differential mode from 9 kHz to 150 kHz, given in 4.12.2 and 4.12.3, are related to disturbance levels between any phase conductor and the neutral conductor measured with a quasi-peak detector and with a bandwidth of 200 Hz in accordance with CISPR 16-1-1. »

Quasi-peak detector is applied on each frequency bin with two time constants when the signal is rising or dropping :

- Fast when the level is rising
- Slow when the level is dropping

Table 3 – Compatibility levels for voltage distortion in differential mode from 9 kHz to 30 kHz[a]

Frequency range kHz	Compatibility levels dB(µV)
9 to 30	129,5 to 122[b]

[a] For EMC coordination in the setting of emission limits for unsymmetrical voltage distortion, see 4.12.1.

[b] The level decreases linearly with the logarithm of the frequency in the range 9 kHz to 30 kHz.

Table 4 – Compatibility levels for voltage distortion in differential mode from 30 kHz to 150 kHz[a]

Frequency range kHz	Compatibility levels dB(µV)
30 to 50[b] 50[b] to 150	122 to 119[c] 113 to 89[c]

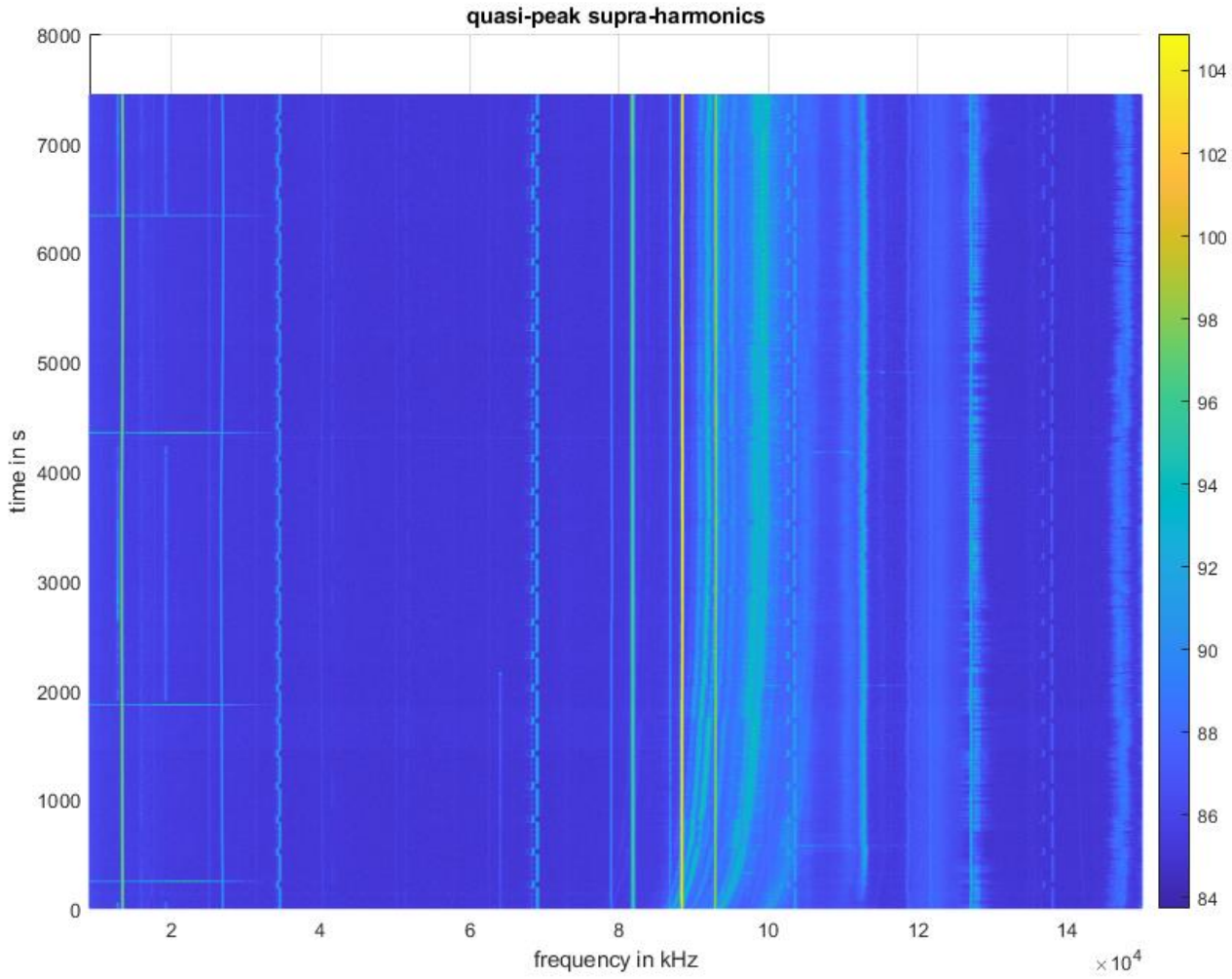
[a] For EMC coordination in the setting of emission limits for unsymmetrical voltage distortion, see 4.12.1.

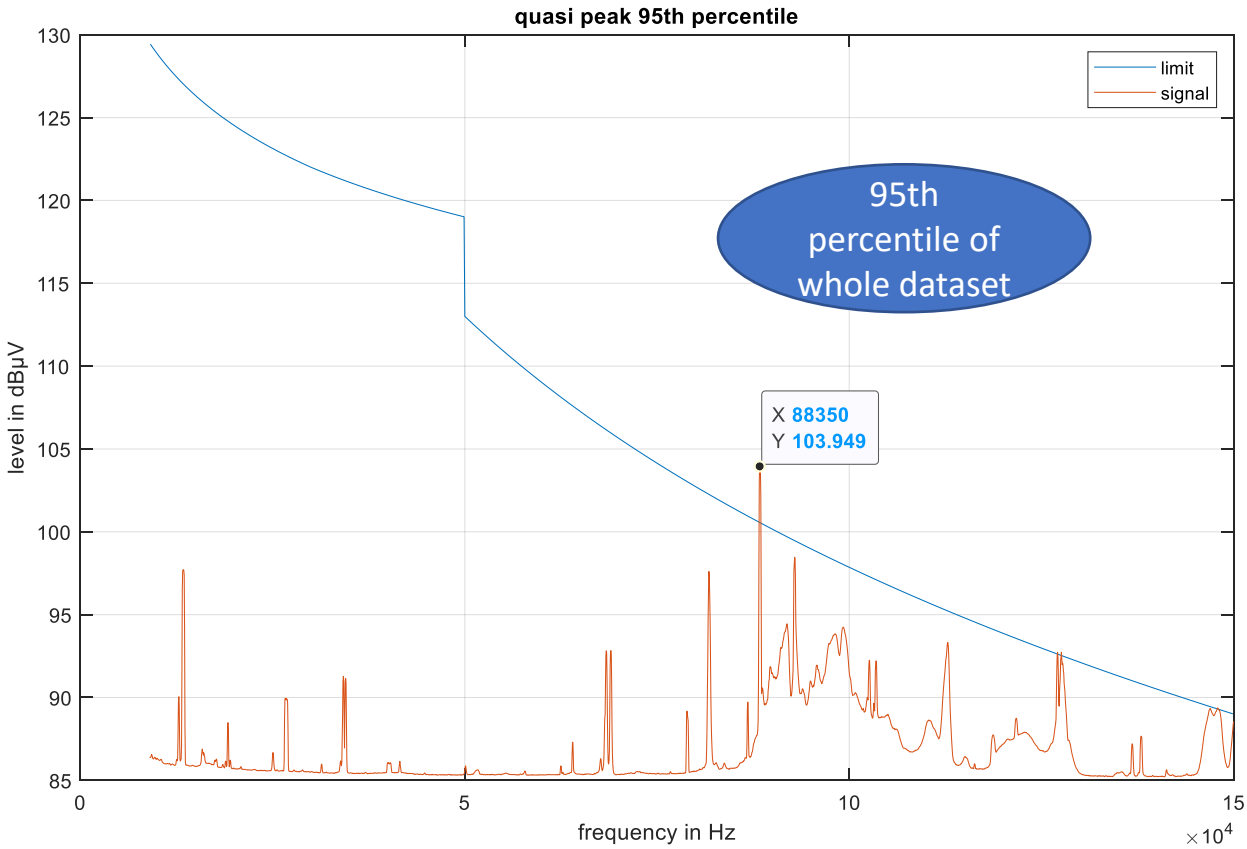
[b] At the transition frequency, the lower level applies.

[c] The level decreases linearly with the logarithm of the frequency in the ranges 30 kHz to 50 kHz and 50 kHz to 150 kHz.

IVL « Integral Voltage Level » is defined in future **IEC 61000-6-3** as a way to assess broadband disturbance, it is similar to **THD** for a specifc frequency band

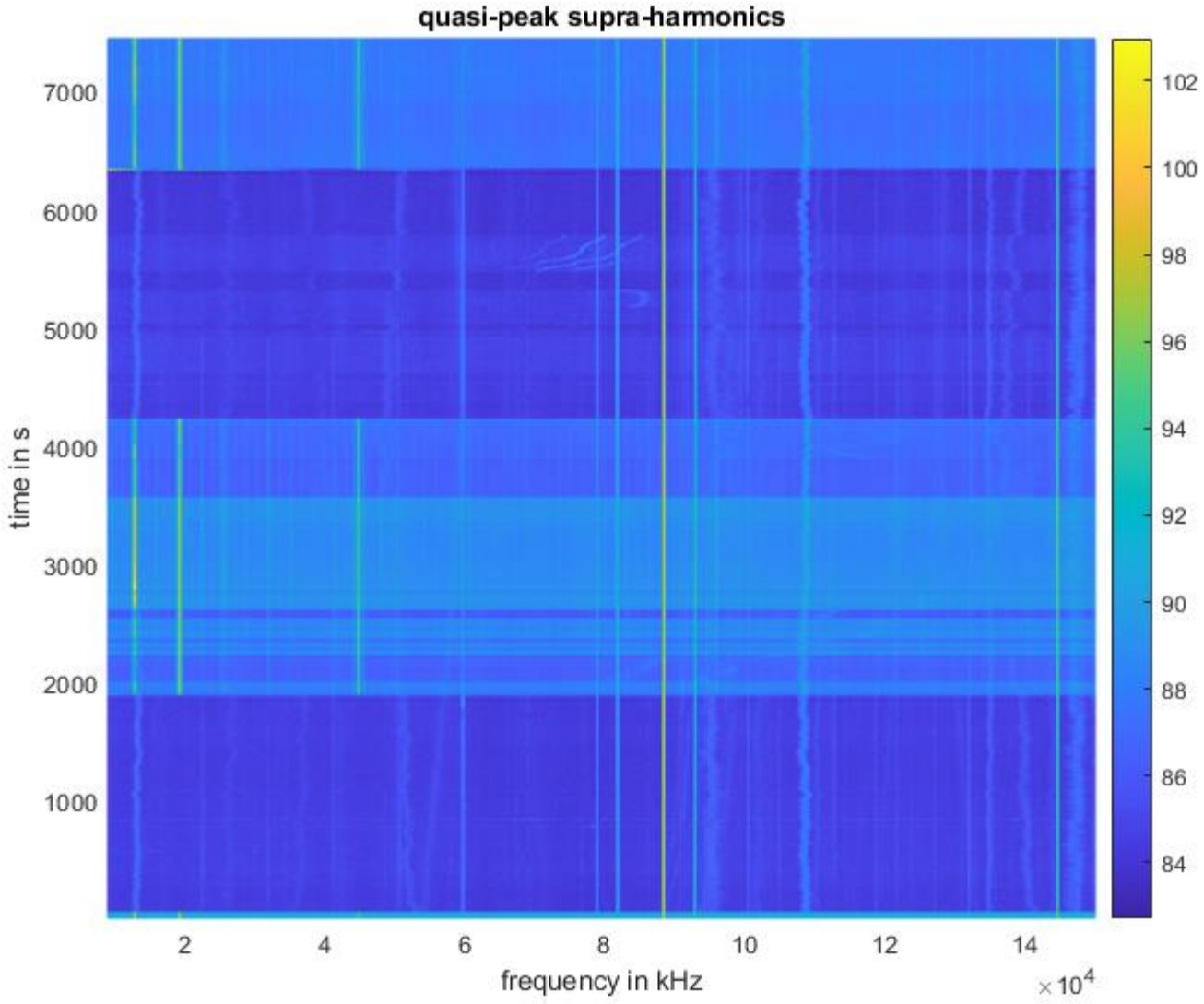
1. Voltage supra-harmonics – time evolution – comparison with compatibility levels

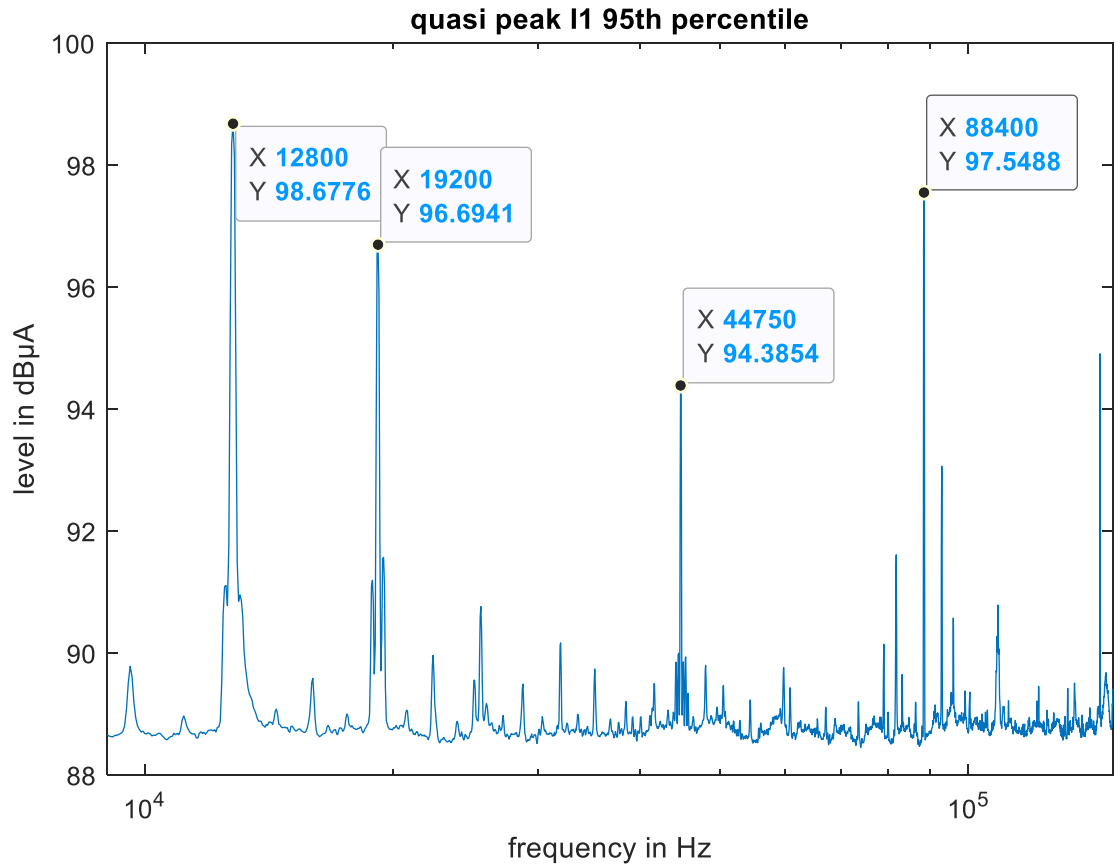




The maximum peak exceed the levels of IEC 61000-2-2 (104dBµV, i.e. about 160mV @88.35 kHz), it could be related with the switching of the AC/DC converter

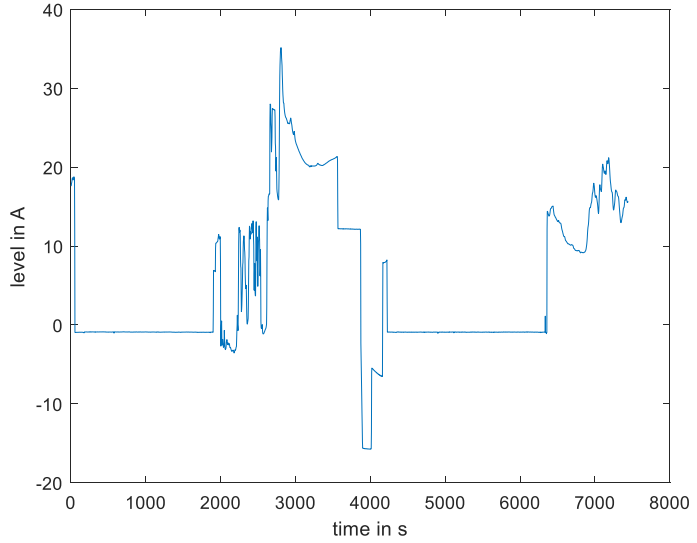
1. Current 1 (ACDC converter) supra-harmonics – time evolution



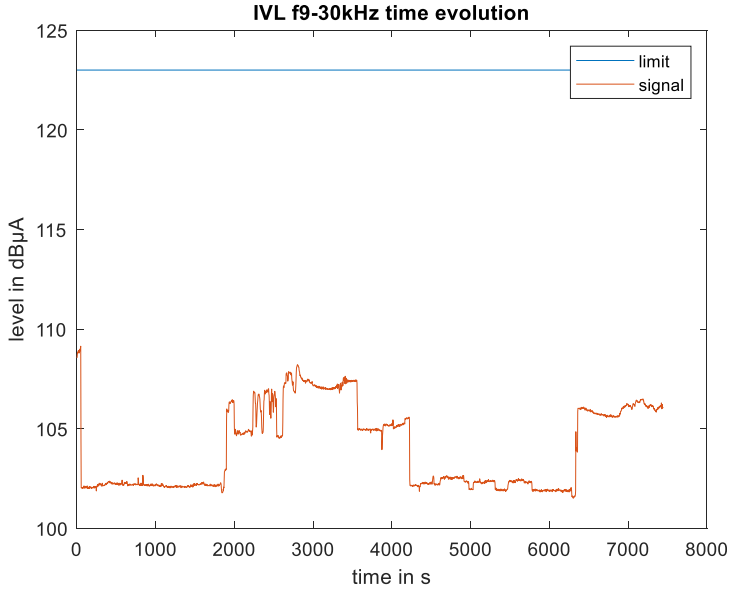


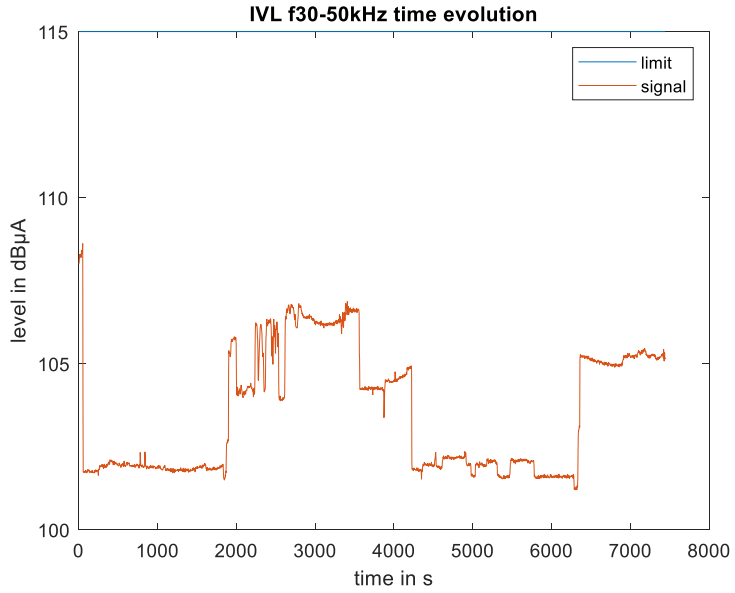
ACDC converter current

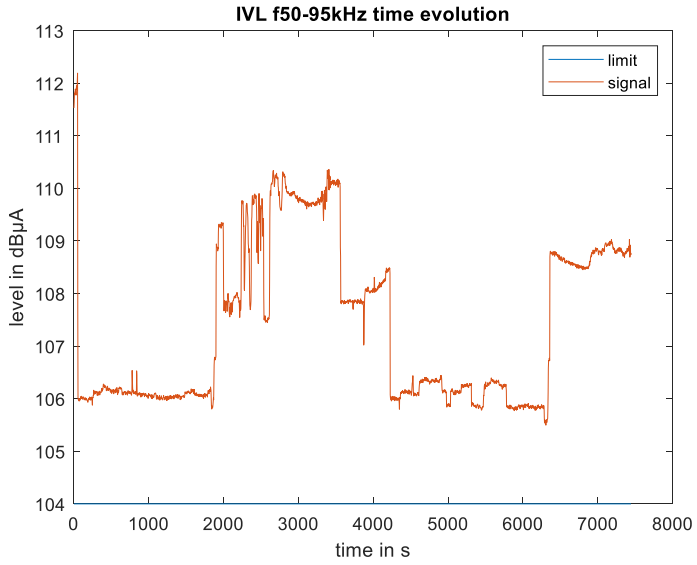
DC value



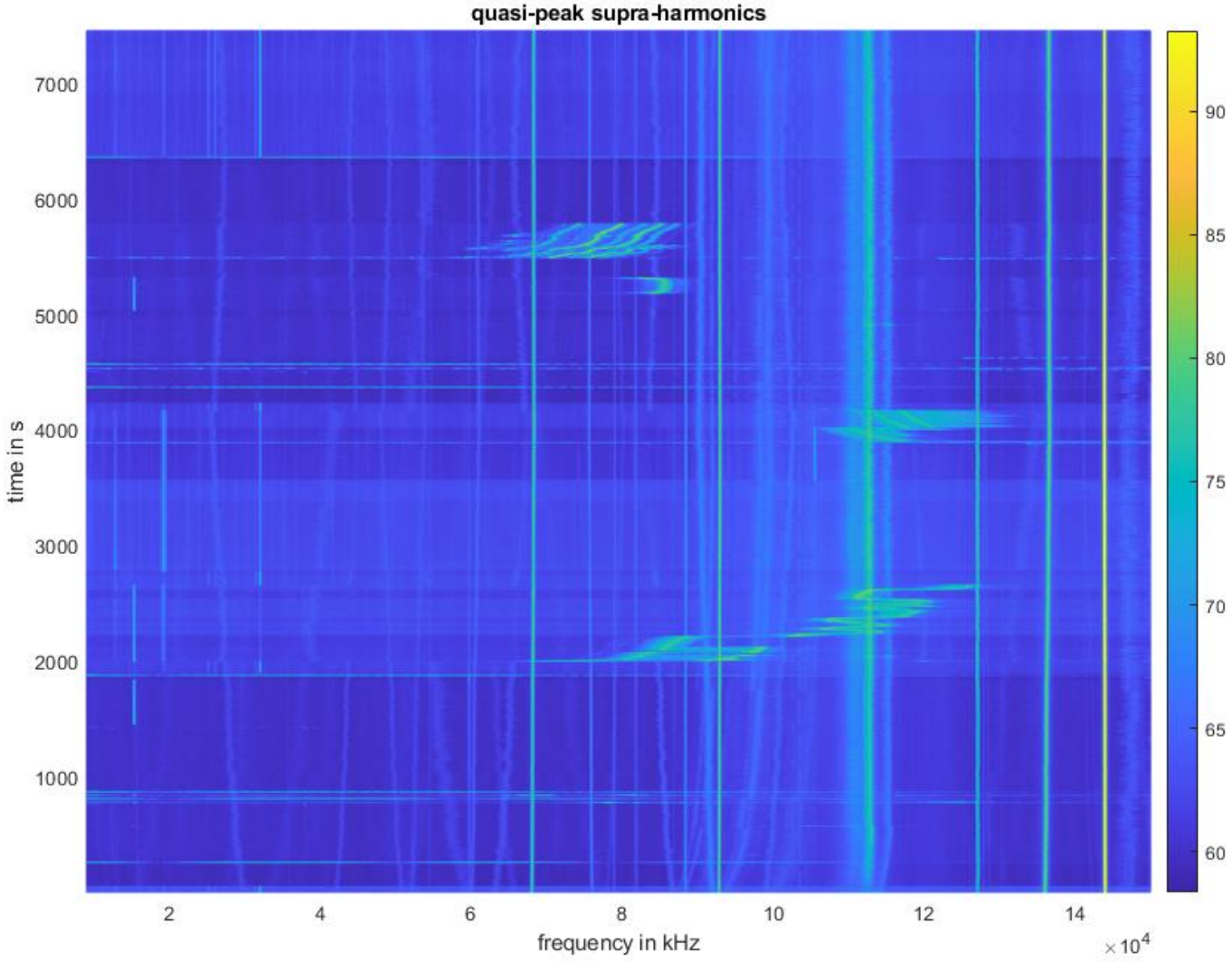
IVL = f(t)

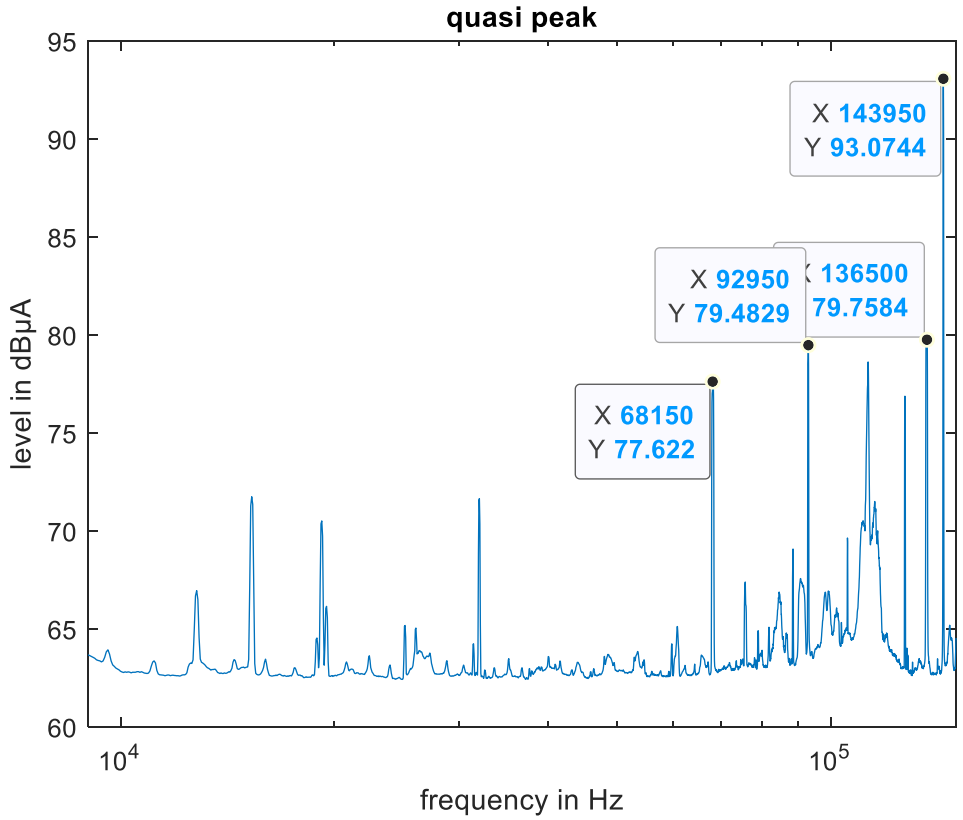






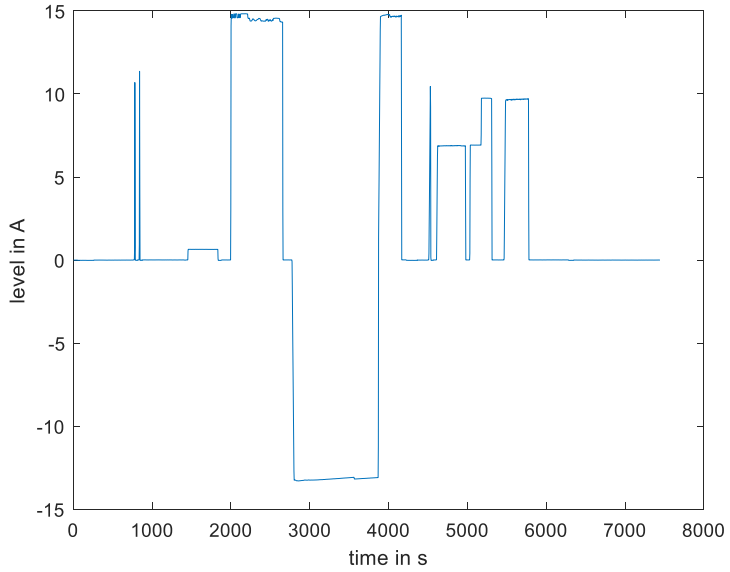
1. Current 2 (EVCS) supra-harmonics – time evolution



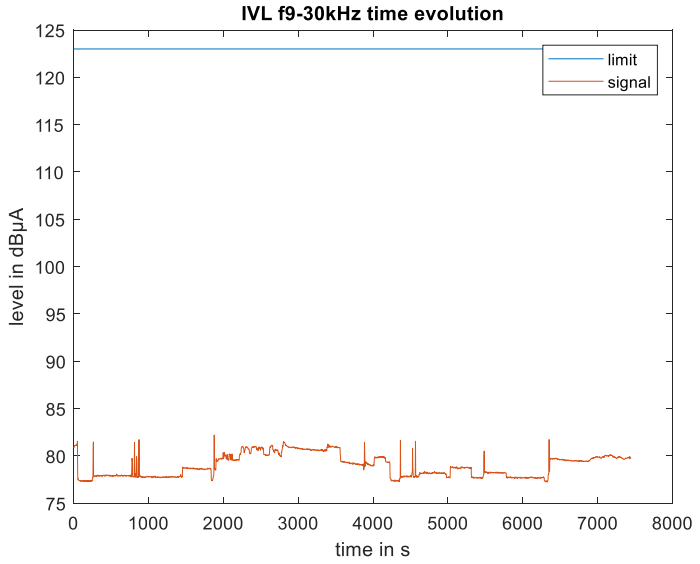


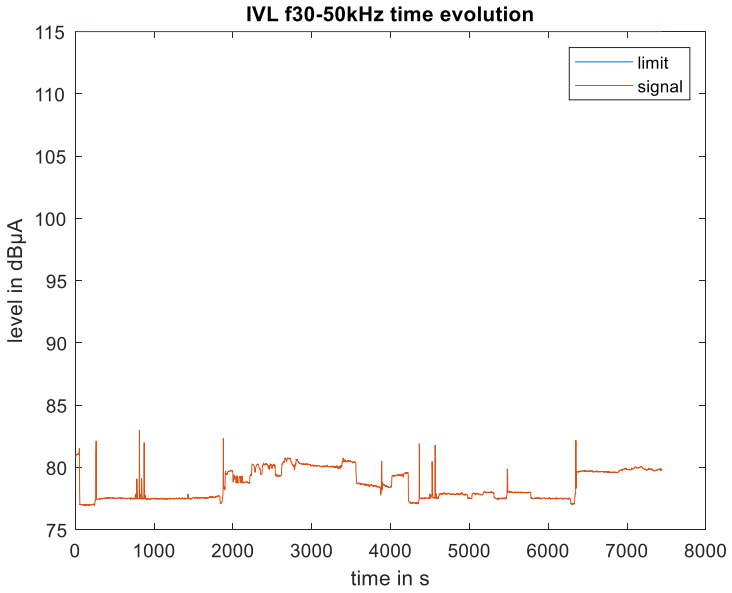
EVCS current

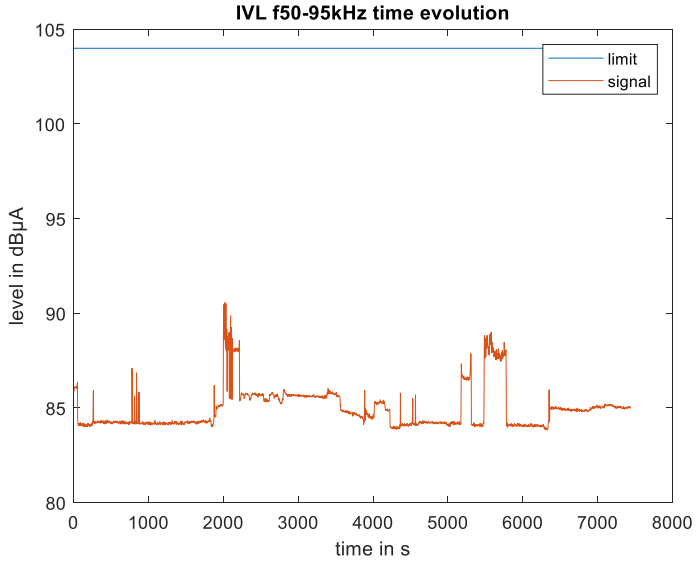
DC value



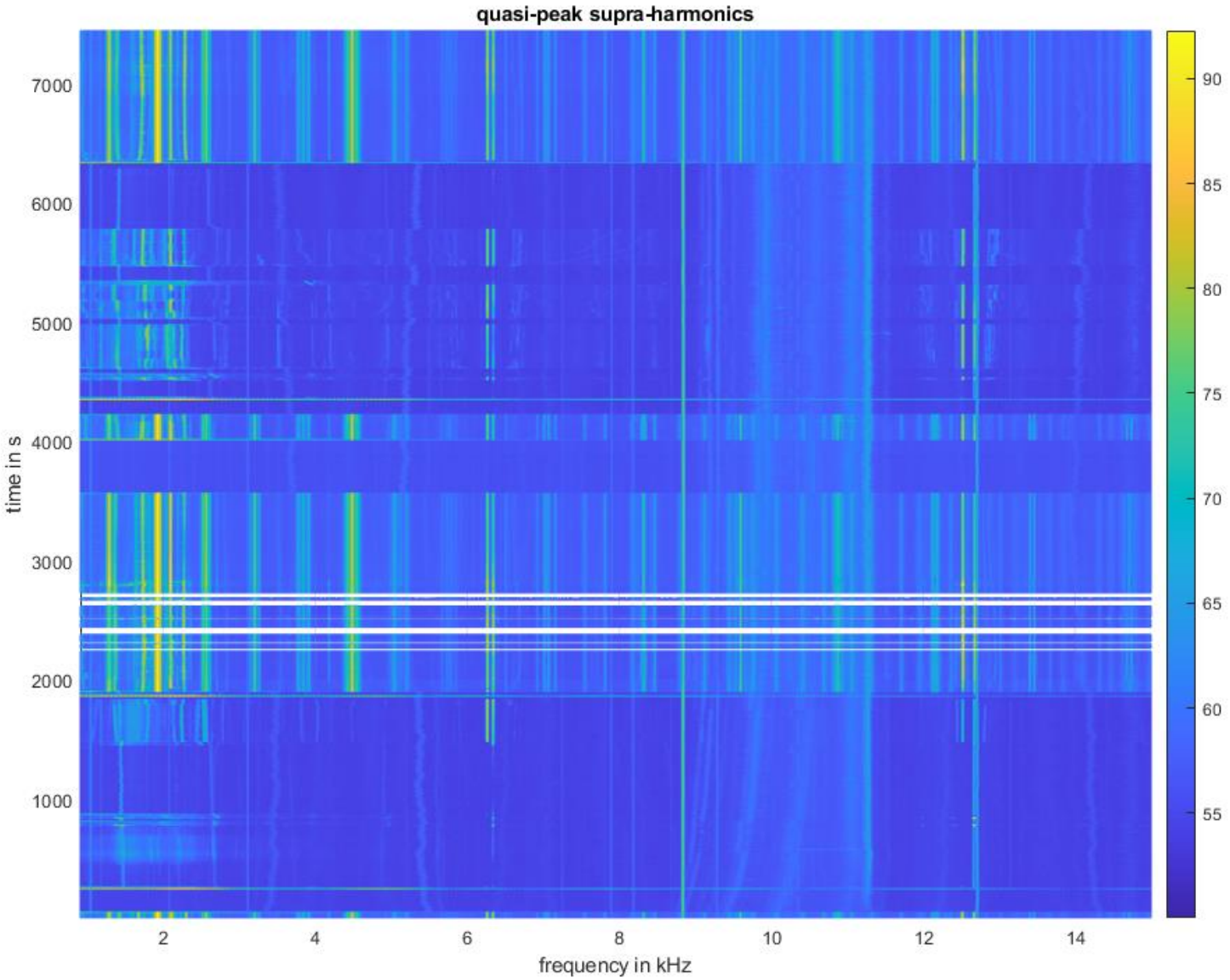
IVL = f(t)

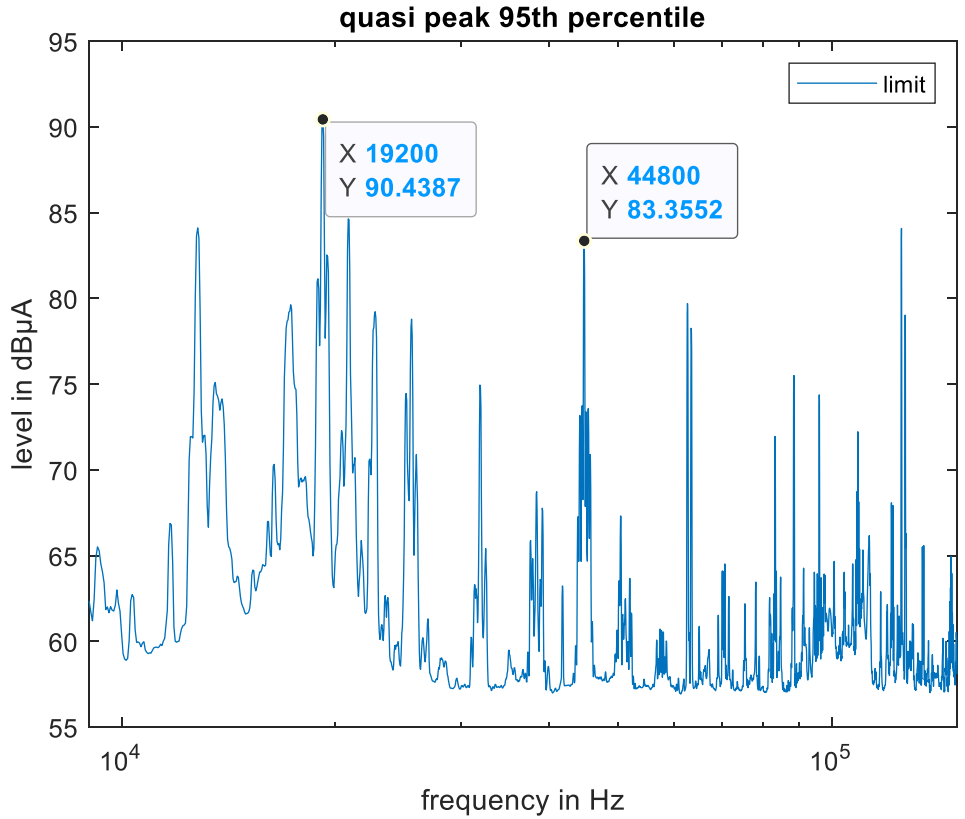




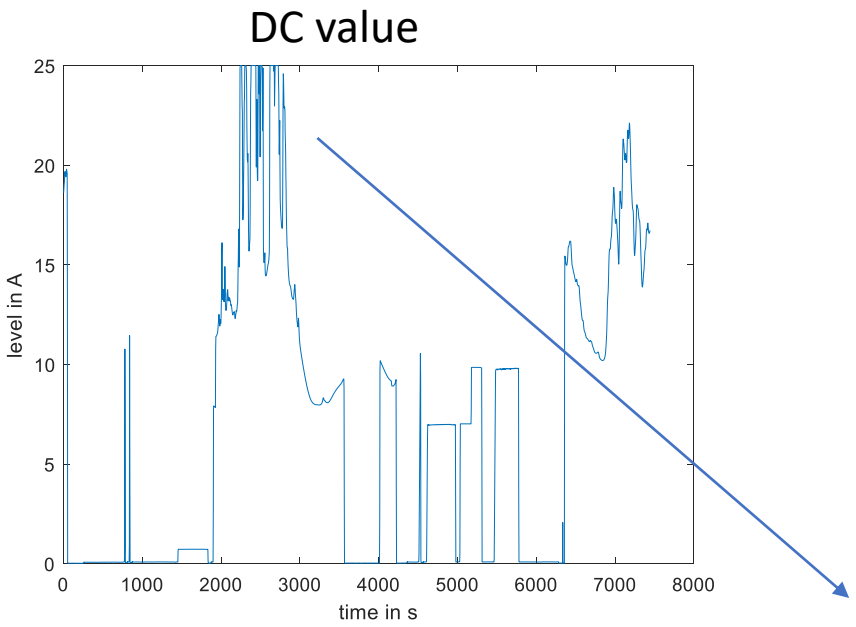


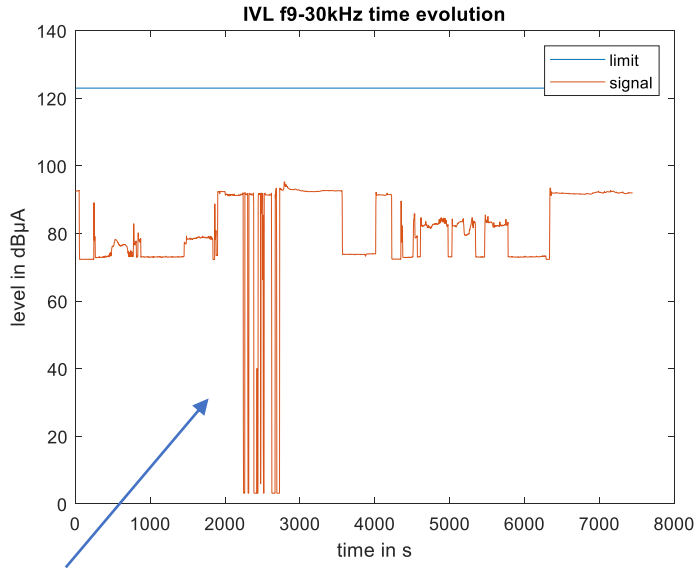
1. Current 3 (PV) supra-harmonics – quasi-peak spectrum



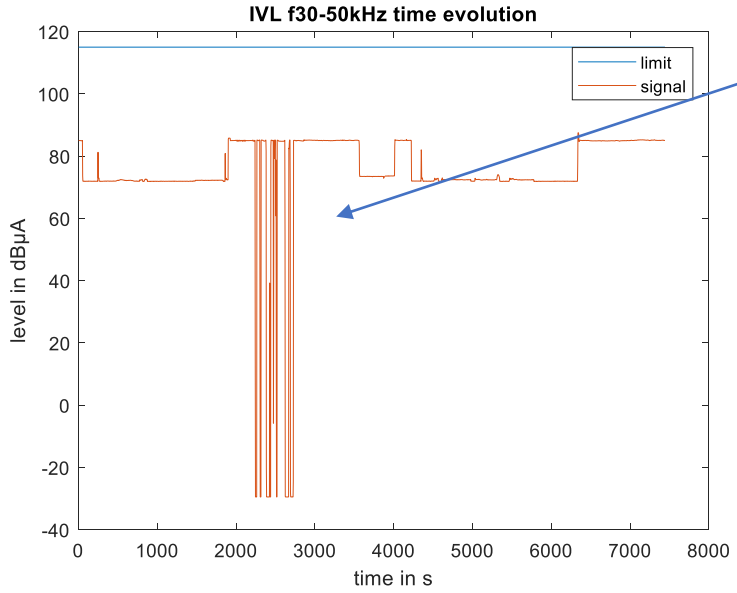


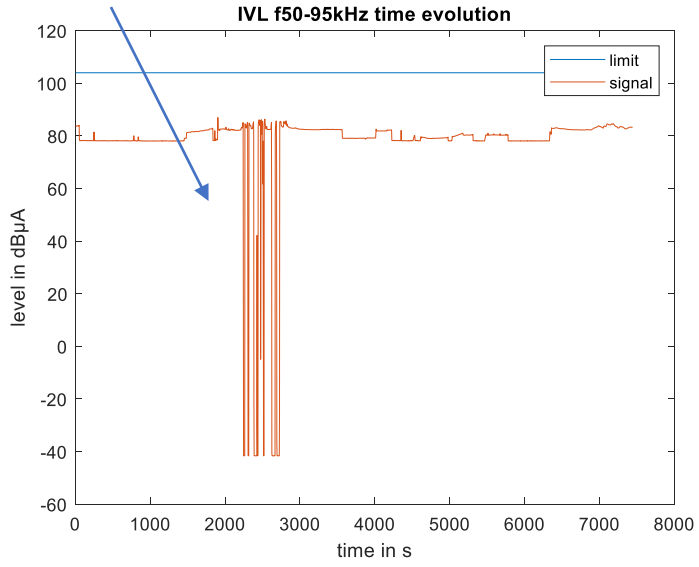
PV current





Error in the calculcations due to the clipping





Thank you